What is claimed is:

1. A dynamic random access memory comprising:

a plurality of memory cell areas arranged in an array, each of which has a plurality of sub word lines, a plurality of bit lines orthogonally intersecting said plurality of sub word lines, and a plurality of dynamic memory cells provided at intersections between said plurality of sub word lines and said plurality of bit lines;

a plurality of first areas, each of which includes a sub word line driving circuit and is arranged between said plurality of memory cell array areas adjacent to each other along the extended direction of said plurality of sub word lines;

a plurality of second areas, each of which includes a sense amplifier circuit and is arranged between said memory array areas adjacent to each other along the extended direction of said plurality of bit lines;

a plurality of third areas, each of which is arranged between said plurality of first areas adjacent to each other;

a plurality of main word lines, each of which is extended over said plurality of first areas

and said plurality of memory cell array areas and is ~~and~~ assigned with two or more sub word lines in each corresponding memory array cell area;

a plurality of first select lines, which are arranged in parallel to said plurality of main word lines to transmit a select signal for selecting one of said two or more sub word lines assigned to a predetermined one of said plurality of main word lines; and

a plurality of second select lines, which are connected to said plurality of first select lines and are extended over adjacent ones of said plurality of first areas via predetermined one of said plurality of third areas to transmit said select signal to said sub word line driving circuit of each of said plurality of first areas adjacent to each other;

wherein one of said plurality of sub word lines assigned to the select main word line is selected by the predetermined sub word line driving circuit that receives a signal from said plurality of second select lines and a signal from said selected main word line.

2. A dynamic random access memory of claim 1, further comprising:

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a plurality of second select line driving circuits, which receive a signal from said plurality of first select lines to drive a corresponding one of said plurality of second select lines;

wherein said plurality of second select line driving circuits are arranged, in a distributed manner, in said plurality of third areas arranged along the extended direction of said plurality of second select lines.

3. A dynamic random access memory of claim 2, wherein each of said plurality of second select lines has a pair of signal lines for transmitting complementary signals, one of said complementary signals being a first signal in phase with the signal received from corresponding one of said plurality of first select lines, the other of said complementary signals being a second signal formed by a corresponding one of said plurality of second select line driving circuits.

4. A dynamic random access memory of claim 3, wherein said sub word line driving circuit includes a first MOSFET of which a gate is connected to a corresponding one of said plurality

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of main word lines and a source-drain path is arranged between the second select line for receiving said second signal and the sub word line.

5. A dynamic random access memory of claim 4, wherein said sub word line driving circuit includes a second MOSFET of which a gate is connected to the second select line for receiving said first signal and of which a source-drain path is arranged between the sub word line and a power supply line.

6. A dynamic random access memory of claim 1, wherein each of said plurality of first select lines is constituted by a pair of signal lines each for transmitting the same signal, said pair of signal lines being arranged to sandwich ~~sandwiching~~ one of said plurality of main word lines.

7. Dynamic random access memory of claim 6, wherein said plurality of select lines and said plurality of main word lines are formed by a first metal layer and said pair of signal lines are short-circuited in said first area by use of a

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second metal layer formed on a layer different from said first metal layer.

8. A dynamic random access memory, comprising:

a main word line;

a plurality of bit line pairs intersecting said main word line;

a plurality of dynamic memory cells;

a plurality of sub word lines each of which has a length equivalent to a ~~the~~ division of said main word line and has the extended direction of said main word line, arranged in plurality toward the direction of the bit line, and connected to address select terminals of said plurality of dynamic memory cells;

a first sub word select line extended in parallel to said main word to transmit a select signal for selecting one of the plurality of sub word lines assigned to said main word line;

a second sub word select line connected to a corresponding one of said first sub word select lines and extended to intersect said main word line;

a plurality of sub word line driving circuits for receiving a ~~the~~ select signal from said

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main word line and ~~the~~ select signal from said second sub word line to form a select signal of said sub word line; and

a plurality of sense amplifier circuits of which input/output pins are connected to said plurality of bit line pairs;

wherein said main word line and said first sub word select line are arranged on a plurality of sub arrays composed of said plurality of sub word lines, said plurality of bit line pairs, and said plurality of dynamic memory cells arranged at intersections between said plurality of sub word lines and said plurality of bit line pairs and said second sub word select line is extended to said sub word driving circuit corresponding to a second sub array adjacent to a first sub array of said plurality of sub arrays to supply the select signal to the corresponding sub word line driving circuit.

9. A dynamic random access memory of claim 8, wherein the sub word line driving circuits are arranged in a divided manner, on both ends of said plurality of sub word line arrays, the sense amplifier circuits are arranged, in a divided manner, on both ends of said plurality of bit line

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pair arrays, and each of said plurality of sub arrays is formed between said plurality of sub word line driving circuit rows and said plurality of sense amplifier circuit rows.

10. A dynamic random access memory of claim 8 or 9, wherein said sense amplifier is based on shared sensing and is provided for the bit lines of the adjacent sub arrays around said sense amplifier and said sub word line driving circuit selects the sub word line of the adjacent sub arrays around said sub word line driving circuit.

11. A dynamic random access memory of claim 8, wherein said main word line is an inverted main word line of which the selected level is the low level and said second sub word select line is composed of a non-inverted sub word select line of which the selected level is the high level and an inverted sub word select line of which the selected level is the low level,

said sub word line driving circuit comprising:

a first complementary metal oxide semiconductor inverter circuit composed of a p-channel MOSFET of which the source is connected

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to said non-inverted sub word select line and an n-channel MOSFET of which the source is connected to ground potential, said main word line being connected to an input terminal composed of the commonly connected gates of these MOSFETs, said sub word line being connected to an output terminal of these MOSFETs; and

an n-channel MOSFET of which a source and drain path is provided between said sub word line and said circuit ground potential and of which a gate is connected to said inverted sub word line;

wherein said inverted sub word line is connected to said first sub word select line and said non-inverted sub word select line is supplied with a select signal formed by an inverter circuit of which an input terminal is connected to said first sub word select line.

12. A dynamic random access memory of claim 11, wherein said inverter circuit is arranged in a cross area where said sense amplifier row and said sub word line driving circuit row intersect.

13. A dynamic random access memory of claim 8, wherein said first sub word select line is formed by use of the same wiring layer as that

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of the main word line and two wiring layers sandwiching one main word line are short-circuited to be used as one first sub word select line.

14. A dynamic random access memory of claim 8, 11, or 12, wherein said main word line and said first sub word select line are formed by a metal layer of a second layer, said second sub word select line is extended using a metal layer of a third layer, the metal layer of said third layer is used at a portion intersecting said main word line, and a metal layer of a first layer is used at a portion connected to a circuit element constituting said sub word line driving circuit.

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